REMARKS

Claims 1 – 15 are pending. Claims 6 – 7 have been withdrawn. New claims 16 – 17 have been added. Applicants respectfully request reconsideration and allowance of this application in view of the above amendments and the following remarks.

The Examiner has objected to the drawings for not showing the limitations of claims 14 and 15. However, as discussed below, Applicants have amended claims 14 and 15 to recite the novel embodiment shown, for example, in Figs. 1 and 2B. Therefore, the objection to the drawings should be withdrawn.

Claims 14 – 15 were rejected under 35 USC 112, second paragraph, as being indefinite. Applicants respectfully request that this rejection be withdrawn for the following reasons.

Claims 14 – 15 recite the novel embodiment disclosed, for example, on pg. 11, lines 1 – 6 in which areas where at least one of the element and the wire is formed below each of the plurality of thin film resistance elements are identical. That is, as shown in Fig. 1 and Fig. 2B, the areas below each of the thin film resistance element are identical.

Therefore, because claims 14 – 15, as amended, recite definite subject matter, the rejection of claims 14 – 15 should be withdrawn.

Claims 6 was rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,194,775 to Usami, with U.S. Patent Pub. No 2001/0053559 to Nagao provided as evidence. Applicants respectfully request that this rejection be withdrawn for the following reasons.

Claim 6, as amended, recites the novel embodiment disclosed, for example, on pgs. 15 - 16 of a semiconductor device having a plurality of thin film resistance elements 30 located above an interlayer insulating film 20 above an area where at least one of an element and a wire 12 is

formed, wherein the interlayer insulting film comprises an inorganic spin-on-glass film 20 formed so as to cover the overall area below an area where the plurality of thin film resistance elements 30 is formed. As shown in, for example, Fig 2B, each of the plurality of thin film resistance elements (L1, L2) has a similar shape.

Usami discloses, in Figs. 2A – 2D, a semiconductor device having a thin film resistance element 209 located above silicon nitride film 208 and BPSG film 207 as an interlayer insulating film. The BPSG film 207 is above an area where an element 204 is formed. However, Usami fails to disclose that a plurality of thin film resistance elements is located above the interlayer insulating film 207. Further, Usami fails to disclose that each of the plurality of thin film resistance elements has a similar shape.

The limitation of a plurality of thin film resistance elements having a similar shape and disposed above the interlayer insulating film leads to improved results that amount to more than a mere design choice. For example, as shown in Fig. 2A, the pairing performance dispersion of the thin film resistance elements can be reduced as a result of the novel embodiment recited in claim 6.

Therefore, because Usami fails to disclose a plurality of thin film resistance elements is located above the interlayer insulating film 207, each of the plurality of thin film resistance elements having a similar shape, it is respectfully requested that the rejection of claim 6 under 35 U.S.C. 102(b) be withdrawn.

Claims 1, 4 and 5 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent No. 6,441,447 to Czagas *et al.* (hereafter: "Czagas"). Applicants respectfully request that this rejection be withdrawn for the following reasons.

Claim 1, as amended, recites the novel embodiment disclosed, for example, on pgs. 11 – 12 of a semiconductor device having a plurality of thin film resistance elements (L1, L2) located above an interlayer insulating film 51 above an area where at least one of an element and a wire 50 is formed on a semiconductor substrate 1. As shown in, for example, Fig. 2C, a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film 51 beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate 1 is set to be within a range that is greater than 0° and less than or equal to 10°. Further, as shown in, for example, Fig. 2B, each of the plurality of thin film resistance elements (L1, L2) has a similar shape.

Czagas discloses, in Fig. 3h, a semiconductor device including a thin film resistor 30 disposed above a dielectric layer 26, which is formed above an area where a wire 22 is formed. The dielectric layer 26 has a connection with another thin film resistor. The wire or aluminum layer 22 is patterned to expose the thin film resistor. The Examiner has asserted that the step or opening provide by exposing the thin film resistor discloses a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be within a range that is greater than 0° and less than or equal to 10°. Applicants respectfully disagree, as the angle of the opening or step is not on the upper surface of the dielectric layer 26. Rather, the step is on the lower surface of the dielectric layer 26.

Further, assuming arguendo that Czagas discloses an angle of a top surface, as admitted by the Examiner, Czagas fails to teach or suggest that angle is greater than 0° and less than or equal to 10°. The Examiner has attempted to cure the deficient teaching of Czagas by arguing that the recited angle range is merely an optimization of a result effective variable. However, a

particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. See MPEP 2144.05 IIB, 8th Ed., Rev. 1, Feb. 2003.

Applicants respectfully request that the Examiner specifically point out the portion of Czagas that teaches or suggests the claimed angle range, cite a reference or references that support this optimization assertion, or withdraw this rejection. Why would the claimed angle range, absent hindsight, be an obvious optimization?

Assuming *arguendo* that Czagas teaches such an angle, Czagas fails to teach or suggest a plurality of thin film resistance elements located above the interlayer insulating film, and that each of the plurality of thin film resistance elements has a similar shape. Rather, Czagas merely discloses a single thin film resistance element 30 above the interlayer insulating film. As discussed above, the limitation of a plurality of thin film resistance elements having a similar shape and disposed above the interlayer insulating film leads to improved results that amount to more than a mere design choice. For example, as shown in Fig. 2A, the pairing performance dispersion of the thin film resistance elements can be reduced.

Therefore, because Czagas fails to teach or suggest: a semiconductor device having a plurality of thin film resistance elements located above an interlayer insulating film above an area where at least one of an element and a wire is formed on a semiconductor substrate, wherein each of the plurality of thin film resistance elements has a similar shape; and a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be within a

range that is greater than 0° and less than or equal to 10°, it is respectfully requested that the rejection of claim 1 be withdrawn.

Claims 4 and 5 depend from claim 1. Therefore, the rejection of these claims should be withdrawn for at least the above-mentioned reasons with respect to claim 1.

Further regarding claim 4, Applicants repeat the above arguments regarding the Examiner's assertion of the claimed wire interval range as optimization of a result-effective variable without establishing that the cited art recognizes the wire interval as a result-effective variable.

Claims 2, 3, 6, 9, 10 and 11 were rejected under 35 USC 103(a) as being unpatentable over Czagas in view of Usami, with Nagao provided as a reference. Applicants respectfully request that this rejection be withdrawn for the following reasons.

Claim 2 recites the novel embodiment disclosed, for example, on pg. 10 in which the interlayer insulating film 20 comprises an inorganic spin-on-glass film formed so as to cover the overall area below the area where the plurality of thin film resistance elements 30 is formed.

As admitted by the Examiner, Czagas fails to disclose that the interlayer insulating film comprises an inorganic spin-on-glass film. Rather, Czagas discloses use of dielectric material such as SiO_2 as the interlayer insulating film. The Examiner has attempted to cure the deficient teaching of Czagas by citing the BPSG of Usami. However, Applicants disagree with the Examiner's assertion that one skilled in the art would be motivated to use the BPSG of Usami rather than the SiO_2 as the dielectric layer, particularly, in view of the conventional use of SiO_2 as an interlevel dielectric because of, for example, its known relative dielectric constant.

However, assuming *arguendo* that one skilled in the art would be motivated to modify Czagas in view of Usami, Czagas in view of Usami still fails to teach or suggest a plurality of

thin film resistance elements located above an interlayer insulating film above an area where at least one of an element and a wire is formed on a semiconductor substrate, wherein each of the plurality of thin film resistance elements has a similar shape, an addition to the limitations of amended claim 1. Accordingly, the rejection of claim 2 under 35 U.S.C. 103(a) should be withdrawn.

Claim 3 recites the novel embodiment disclosed, for example, on pgs. 19 – 20, and shown in, for example, Fig. 6, in which the interlayer insulating film comprises an inorganic spin-on-glass film, and wherein an upper surface of the interlayer insulating film has a higher area adjacent to an area where the plurality of thin film resistance elements is formed than in the area where the plurality of thin film resistance elements is not formed. A high step can be formed in the periphery of the thin film resistance elements because the SOG is easily collected thereunder.

Czagas discloses an interlayer insulating film 26 below a thin film resistor 30 (See Fig. 3h). However, Czagas fails to teach or suggest that the an upper surface of the interlayer insulating film has a higher area adjacent to an area where the thin film resistance element is formed than in the area where the thin film resistance element is not formed. Therefore, the rejection of claim 3 under 35 U.S.C. 103(a) should be withdrawn.

Claim 6, as amended, recites the novel embodiment disclosed, for example, on pgs. 15 – 16 of a semiconductor device having a plurality of thin film resistance elements 30 located above an interlayer insulating film 20 above an area where at least one of an element and a wire 12 is formed, wherein the interlayer insulting film comprises an inorganic spin-on-glass film 20 formed so as to cover the overall area below an area where the plurality of thin film resistance elements 30 is formed. As shown in, for example, Fig 2B, each of the plurality of thin film resistance elements (L1, L2) has a similar shape.

Czagas discloses, in Fig. 3h, a semiconductor device including a thin film resistor 30 disposed above a dielectric layer 26, which is formed above an area where a wire 22 is formed. The dielectric layer 26 has a connection with another thin film resistor. The wire or aluminum layer 22 is patterned to expose the thin film resistor.

However, Czagas fails to teach or suggest a plurality of thin film resistance elements located above the interlayer insulating film, and that each of the plurality of thin film resistance elements has a similar shape. Rather, Czagas merely discloses a single thin film resistance element 30 above the interlayer insulating film. As discussed above, the limitation of a plurality of thin film resistance elements having a similar shape and disposed above the interlayer insulating film leads to improved results that amount to more than a mere design choice. For example, as shown in Fig. 2A, the pairing performance dispersion of the thin film resistance elements can be reduced.

Therefore, because Czagas fails to teach or suggest a plurality of thin film resistance elements located above the interlayer insulating film, and that each of the plurality of thin film resistance elements has a similar shape, the rejection of claim 6 under 35 U.S.C. 103(a) should be withdrawn.

Claim 9, as amended, recites the novel embodiment disclosed, for example, on pgs. 13 – 15 of a semiconductor device having a plurality of thin film resistance elements 30 disposed above an interlayer insulating film above an area where at least one of an element and a wire is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film 20 beneath an area where plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be greater than 0° and less than or equal to 10°,

wherein the interlayer insulating film comprises an inorganic spin-on-glass film formed so as to cover the overall area below the area where the thin film resistance element is formed, wherein the plurality of thin film resistance elements is formed on an area where the wire is formed, and a wire interval is set to 1.7μm or more, wherein each of the plurality of thin film resistance elements has a similar shape.

Czagas discloses, in Fig. 3h, a semiconductor device including a thin film resistor 30 disposed above a dielectric layer 26, which is formed above an area where a wire 22 is formed. The dielectric layer 26 has a connection with another thin film resistor. The wire or aluminum layer 22 is patterned to expose the thin film resistor.

However, Czagas fails to teach or suggest a plurality of thin film resistance elements located above the interlayer insulating film, and that each of the plurality of thin film resistance elements has a similar shape. Rather, Czagas merely discloses a single thin film resistance element 30 above the interlayer insulating film. As discussed above, the limitation of a plurality of thin film resistance elements having a similar shape and disposed above the interlayer insulating film leads to improved results that amount to more than a mere design choice. For example, as shown in Fig. 2A, the pairing performance dispersion of the thin film resistance elements can be reduced.

Further, Czagas fails to teach or suggest the recited angle greater than 0° and less than or equal to 10° or that a wire interval is set to 1.7μm or more. The Examiner has attempted to cure the deficient teaching of Czagas by arguing that the angle and wire intervals are result effective variables. However, a particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or

workable ranges of said variable might be characterized as routine experimentation. See MPEP 2144.05 IIB, 8th Ed., Rev. 1, Feb. 2003.

Applicants respectfully request that the Examiner specifically point out the portion of Czagas that teaches or suggests the claimed angle range and wire interval range, cite a reference or references that support this optimization assertion, or withdraw this rejection.

The Examiner asserted in response to Applicants' previous arguments that Fig. 2A does not show the criticality of 10 degrees. However, as clearly discussed on pg. 13, and as shown in Fig. 2A, the dispersion of pairing performance increases sharply at and after the stage that the taper angle exceeds 10 degrees. That is, an angle of less than 10 degrees can achieve a stabilized pair performance even the interlayer insulation layer is uneven. Further, although this value range was sampled from experimental results, Applicants still assert that Fig. 2 shows the criticality of 10 degrees.

Regarding the rejection of claims 10 and 11, these claims depend from claims 3 and 9, respectively. Therefore, the rejection of these claims should be withdrawn for at least the above-mentioned reasons with respect to claims 3 and 9. Further regarding claims 3 and 9, Applicants repeat the above arguments regarding the Examiner's assertion of the claimed resistor width as optimization of a result-effective variable without establishing that the cited art recognizes the width of the resistor as a result-effective variable.

Claims 1 – 2, 4 – 6, 9, 10 and 12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Nagao. Applicants respectfully request that this rejection be withdrawn for the following reasons.

Claim 1, as amended, recites the novel embodiment disclosed, for example, on pgs. 11 – 12 of a semiconductor device having a plurality of thin film resistance elements (L1, L2) located

above an interlayer insulating film 51 above an area where at least one of an element and a wire 50 is formed on a semiconductor substrate 1. As shown in, for example, Fig. 2C, a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film 51 beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate 1 is set to be within a range that is greater than 0° and less than or equal to 10°. Further, as shown in, for example, Fig. 2B, each of the plurality of thin film resistance elements (L1, L2) has a similar shape.

Nagao discloses a matrix substrate in which a pixel electrode 111 is formed over first and second leveling films 109, 110, which is above an area where a wiring 107 is formed on a semiconductor substrate 100. However, Nagao fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape. Rather, Nagao merely discloses a pixel electrode 111 on the leveling film 109. Further, contrary to the contention of the Examiner, the pixel electrode 111 fails to teach or suggest a thin film resistance element. Rather, Nagao discloses that the pixel electrode 722 can be transparent conductive film or metal film. (See pg. 6, paragraph [0086]).

Therefore, because Nagao fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape, the rejection of claim 1 under 35 U.S.C. 103(a) should be withdrawn.

Claims 2, 4 and 5 depend from claim 1. Therefore, the rejection of these claims should be withdrawn for at least the above-mentioned reasons with respect to claim 1.

Claim 6, as amended, recites the novel embodiment disclosed, for example, on pgs. 15 - 16 of a semiconductor device having a plurality of thin film resistance elements 30 located above an interlayer insulating film 20 above an area where at least one of an element and a wire 12 is formed, wherein the interlayer insulting film comprises an inorganic spin-on-glass film 20 formed so as to cover the overall area below an area where the plurality of thin film resistance elements 30 is formed. As shown in, for example, Fig 2B, each of the plurality of thin film resistance elements (L1, L2) has a similar shape.

As discussed above, Nagao discloses a matrix substrate in which a pixel electrode 111 is formed over first and second leveling films 109, 110, which is above an area where a wiring 107 is formed on a semiconductor substrate 100. However, Nagao fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape. Rather, Nagao merely discloses a pixel electrode 111 on the leveling film 109.

Therefore, because Nagao fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape, the rejection of claim 6 under 35 U.S.C. 103(a) should be withdrawn.

Claim 9, as amended, recites the novel embodiment disclosed, for example, on pgs. 13 – 15 of a semiconductor device having a plurality of thin film resistance elements 30 disposed above an interlayer insulating film above an area where at least one of an element and a wire is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film 20 beneath an area where plurality of thin film resistance elements is formed intersects to the

surface of the semiconductor substrate is set to be greater than 0° and less than or equal to 10°, wherein the interlayer insulating film comprises an inorganic spin-on-glass film formed so as to cover the overall area below the area where the thin film resistance element is formed, wherein the plurality of thin film resistance elements is formed on an area where the wire is formed, and a wire interval is set to 1.7μm or more, wherein each of the plurality of thin film resistance elements has a similar shape.

As discussed above, Nagao discloses a matrix substrate in which a pixel electrode 111 is formed over first and second leveling films 109, 110, which is above an area where a wiring 107 is formed on a semiconductor substrate 100. However, Nagao fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape. Rather, Nagao merely discloses a pixel electrode 111 on the leveling film 109. Accordingly, the rejection of claim 9 under 35 U.S.C. 103(a) should be withdrawn.

Regarding the rejection of claim 10, claim 10 depends from claim 9. Therefore, the rejection of claim 10 should be withdrawn for at least the above-mentioned reasons with respect to claim 9.

Claim 12, as amended, recites the novel embodiment disclosed, for example, on pgs. 11 – 12 of a semiconductor device having a plurality of thin film resistance elements (L1, L2) disposed above an interlayer insulating film 51 above an area where a plurality of wires 50 is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be greater than 0° and less than or equal to 10°,

wherein the interlayer insulating film comprises an inorganic spin-on-glass film, wherein a wire interval is set to 1.7μm or more, wherein each of the plurality of thin film resistance elements has a similar shape.

As discussed above, Nagao discloses a matrix substrate in which a pixel electrode 111 is formed over first and second leveling films 109, 110, which is above an area where a wiring 107 is formed on a semiconductor substrate 100. However, Nagao fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape. Rather, Nagao merely discloses a pixel electrode 111 on the leveling film 109. Accordingly, the rejection of claim 12 under 35 U.S.C. 103(a) should be withdrawn.

Claims 1, 3, 5, 6 and 9 – 13 have been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. No. 2002/0020879 to Shiiki *et al.* (hereafter: "Shiiki") in view of Nagao. Applicants respectfully request that this rejection be withdrawn for the following reasons.

Claim 1, as amended, recites the novel embodiment disclosed, for example, on pgs. 11 – 12 of a semiconductor device having a plurality of thin film resistance elements (L1, L2) located above an interlayer insulating film 51 above an area where at least one of an element and a wire 50 is formed on a semiconductor substrate 1. As shown in, for example, Fig. 2C, a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film 51 beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate 1 is set to be within a range that is greater than 0° and less than or equal to 10°. Further, as shown in, for example, Fig. 2B, each of the plurality of thin film resistance elements (L1, L2) has a similar shape.

Shiiki discloses a substrate in which a resistor 2 is formed over interlayer insulating film 3, which is above an area where a wiring 7 is formed on a semiconductor substrate. However, Shiiki fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape. Rather, Shiiki merely discloses a resistor 2 on the interlayer insulating film 3.

Further, as admitted by the Examiner, Shiiki fails to teach or suggest that a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be within a range that is greater than 0° and less than or equal to 10°.

The Examiner has asserted that one skilled in the art would be motivated to use the first and second leveling films 109, 110 taught by Nagao as the interlaying insulating film in Shiiki for the purpose of achieving a flat surface without requiring additional planarization steps. Applicants respectfully disagree because (1) Shiiki already discloses achieving a flat surface by CMP; and (2) the flattening process disclosed in Nagao discloses using first and second leveling films 109, 110 (See, for example, Fig. 4 of Nagao). Why would one skilled in the art be motivated to use the first and second leveling films 109, 110 of Nagao rather than CMP disclosed in Shiiki when Shiiki already appears to achieve a flat surface? Further, Nagao requires the user of multiple leveling films to achieve the flat surface. Therefore, no "additional step" would be avoided by use of Nagao.

Therefore, because Shiiki fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape, and that a taper angle at which a line connecting the

local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be within a range that is greater than 0° and less than or equal to 10°, the rejection of claim 1 under 35 U.S.C. 103(a) should be withdrawn.

Claims 3 and 5 depend from claim 1. Therefore, the rejection of claims 3 and 5 should be withdrawn for at least the above-mentioned reasons with respect to claim 1.

Further regarding claim 3, claim 3 recites the novel embodiment disclosed, for example, on pgs. 19 – 20, and shown in, for example, Fig. 6, in which the interlayer insulating film comprises an inorganic spin-on-glass film, and wherein an upper surface of the interlayer insulating film has a higher area adjacent to an area where the plurality of thin film resistance elements is formed than in the area where the plurality of thin film resistance elements is not formed.

Shiiki fails to teach or suggest that an upper surface of the interlayer insulating film 3 has a higher area adjacent to an area where the thin film resistance element 2 is formed than in the area where the thin film resistance element 2 is not formed.

The Examiner has asserted that "since the step in the insulating film is formed as a result of the underlying wiring 6, and that wiring is located under the resistance element, it follows that an upper surface of the interlayer insulating film has a higher area adjacent to an area where the thin film resistance element is formed than an areas where the resistance element is not formed. An electrode 4 and interlayer insulating film 5 are located adjacent to and under the resistance element. So, by the Examiner's same logic, the adjacent area should not be higher because it follows that an uppers surface above the electrode 4 and interlayer insulating film 5 as well should be higher.

Therefore, because Shiiki fails to teach or suggest that an upper surface of the interlayer insulating film 3 has a higher area adjacent to an area where the thin film resistance element 2 is formed than in the area where the thin film resistance element 2 is not formed, it is respectfully requested that the rejection of claim 3 under 35 U.S.C. 103(a) be withdrawn.

Claim 6, as amended, recites the novel embodiment disclosed, for example, on pgs. 15 – 16 of a semiconductor device having a plurality of thin film resistance elements 30 located above an interlayer insulating film 20 above an area where at least one of an element and a wire 12 is formed, wherein the interlayer insulting film comprises an inorganic spin-on-glass film 20 formed so as to cover the overall area below an area where the plurality of thin film resistance elements 30 is formed. As shown in, for example, Fig 2B, each of the plurality of thin film resistance elements (L1, L2) has a similar shape.

Shiiki discloses a substrate in which a resistor 2 is formed over interlayer insulating film 3, which is above an area where a wiring 7 is formed on a semiconductor substrate. However, Shiiki fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape. Rather, Shiiki merely discloses a resistor 2 on the interlayer insulating film 3. Accordingly, the rejection of claim 6 under 35 U.S.C. 103(a) should be withdrawn.

Claim 9, as amended, recites the novel embodiment disclosed, for example, on pgs. 13 – 15 of a semiconductor device having a plurality of thin film resistance elements 30 disposed above an interlayer insulating film above an area where at least one of an element and a wire is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film 20 beneath an area where plurality of thin film resistance elements is formed intersects to the

surface of the semiconductor substrate is set to be greater than 0° and less than or equal to 10°, wherein the interlayer insulating film comprises an inorganic spin-on-glass film formed so as to cover the overall area below the area where the thin film resistance element is formed, wherein the plurality of thin film resistance elements is formed on an area where the wire is formed, and a wire interval is set to 1.7μm or more, wherein each of the plurality of thin film resistance elements has a similar shape.

Shiiki discloses a substrate in which a resistor 2 is formed over interlayer insulating film 3, which is above an area where a wiring 7 is formed on a semiconductor substrate. However, Shiiki fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape. Rather, Shiiki merely discloses a resistor 2 on the interlayer insulating film 3. Further, Shiiki fails to teach or suggest that a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be within a range that is greater than 0° and less than or equal to 10°. Accordingly, the rejection of claim 9 should be withdrawn.

Regarding the rejection of claim 10, claim 10 depends from claim 9. Therefore, the rejection of claim 10 should be withdrawn for at least the above-mentioned reasons with respect to claim 9.

Regarding the rejection of claim 11, claim 11 depends from claim 3. Therefore, the rejection of claim 11 should be withdrawn for at least the above-mentioned reasons with respect to claim 3.

Claim 12, as amended, recites the novel embodiment disclosed, for example, on pgs. 11 – 12 of a semiconductor device having a plurality of thin film resistance elements (L1, L2) disposed above an interlayer insulating film 51 above an area where a plurality of wires 50 is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be greater than 0° and less than or equal to 10°, wherein the interlayer insulating film comprises an inorganic spin-on-glass film, wherein a wire interval is set to 1.7μm or more, wherein each of the plurality of thin film resistance elements has a similar shape.

Shiiki discloses a substrate in which a resistor 2 is formed over interlayer insulating film 3, which is above an area where a wiring 7 is formed on a semiconductor substrate. However, Shiiki fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape. Rather, Shiiki merely discloses a resistor 2 on the interlayer insulating film 3. Further, Shiiki fails to teach or suggest that a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be within a range that is greater than 0° and less than or equal to 10°. Accordingly, the rejection of claim 12 under 35 U.S.C. 103(a) should be withdrawn.

Claim 13 depends from claim 1. Therefore, the rejection of claim 13 should be withdrawn for the above-mentioned reasons with respect to claim 1.

New claims 16 – 17 are presented for examination. Support for these claims can be found on, for example, pg. 10, line 19.

In view of the foregoing, the applicants submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

If there are any problems with the payment of fees, please charge any underpayments and credit any overpayments to Deposit Account No. 50-1147.

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